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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,581	10/30/2003	Takashi Noma	492322014500	7231

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,581	NOMA ET AL	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3,6,7,12,13 and 15* is/are allowed.

6)☒ Claim(s) *1,4,5,8-11,14 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities. Appropriate correction is required.

► In claim 1,

line 2, after "a semiconductor" insert --wafer--.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 16, 17 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

► With respect to claims 16-18, the phrase "forming a photoresist layer by spray coating" renders the claim indefinite. It is not clear where the photoresit layer is formed on.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 16-18, as best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant Admitted Prior Art (fig. 12, page. 2).

Applicant Admitted Prior Art discloses (fig. 12, page. 2) a manufacturing method of a semiconductor device, comprising:

bonding a first supporting substrate (102) to a top surface of a semiconductor wafer (104), a first wiring (107) being formed on the top surface;

dividing the semiconductor wafer (104) into a plurality of semiconductor dice by etching the semiconductor wafer (104) along a dicing line from a back surface of the semiconductor wafer (104);

bonding a second supporting substrate (103) to a back surfaces of the plurality of semiconductor dice through a resin layer (105a);

forming a groove to expose a portion of the first wiring by cutting the second supporting substrate (103), the resin layer (105a), and the first supporting substrate (102) along the dicing line from a surface of the second supporting substrate, the groove reaching inside the first supporting substrate;

forming a second wiring (110) connected to the exposed portion of the first wiring (107) and extending over the surface of the second supporting substrate (103);

forming a protection film comprising an organic resin (epoxy resin) on a surface of the second wiring; and

forming an opening (the location of a ball shaped conductive terminal 106) in the protection film at a predetermined position to expose the second wiring (110).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-5, 8-11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (fig. 12, page. 2) in view of Tanaka [U.S. Pat. 6,753,936].

► With respect to claims 1 and 10, Applicant Admitted Prior Art discloses (fig. 12, page. 2) a manufacturing method of a semiconductor device, comprising:

bonding a first supporting substrate (102) to a top surface of a semiconductor wafer (104), a first wiring (107) being formed on the top surface;

bonding a second supporting substrate (103) to a back surface of the semiconductor wafer (104);

forming a groove to expose a portion of the first wiring by cutting the second supporting substrate (103), the semiconductor wafer (104) and the first supporting

substrate (102) from a surface of the second supporting substrate, the groove reaching inside the first supporting substrate;

forming a second wiring (110) connected to the exposed portion of the first wiring (107) and extending over the surface of the second supporting substrate (103);

forming a protection film comprising an organic resin (epoxy resin) on a surface of the second wiring; and

forming an opening (the location of a ball shaped conductive terminal 106) in the protection film at a predetermined position to expose the second wiring (110).

Applicant Admitted Prior Art fails to disclose forming the protection film (epoxy resin) by spray coating method. However, Tanaka discloses that the protection film (epoxy resin) (119C) can be formed by spray coating method (see fig. 20, col. 13, lines 27-31).

Therefore, at the time of invention, it would have been obvious to the skilled in the art to use spray coating method as taught by Tanaka into the process of Applicant Admitted Prior Art because the spray coating is easy to control and well coated with even surface.

► With respect to claims 4, 8 and 14, Applicant Admitted Prior Art (fig. 12) discloses that forming a conductive terminal (106) on the second wiring exposed through the opening in the protection film (111).

► With respect to claims 5 and 10, Applicant Admitted Prior Art discloses (fig. 12, page. 2) a manufacturing method of a semiconductor device, comprising:

bonding a supporting substrate (102) to a top surface of a semiconductor wafer (104), a first wiring (107) being formed on the top surface;

forming a groove to expose a portion of the first wiring by etching the semiconductor wafer (104) from a back surface of the semiconductor wafer (104);

forming a second wiring (110) connected to the exposed portion of the first wiring (107) and extending over the back surface of the semiconductor wafer (104);

forming a protection film comprising an organic resin (epoxy resin) on a surface of the second wiring; and

forming an opening (the location of a ball shaped conductive terminal 106) in the protection film at a predetermined position to expose the second wiring (110).

Applicant Admitted Prior Art fails to disclose forming the protection film (epoxy resin) by spray coating method. However, Tanaka discloses that the protection film (epoxy resin) (119C) can be formed by spray coating method (see fig. 20, col. 13, lines 27-31). Therefore, it would have been obvious to the skilled in the art to use spray coating method as taught by Tanaka into the process of Applicant Admitted Prior Art because the spray coating is easy to control and well coated with even surface.

► With respect to claim 9, Applicant Admitted Prior Art (page 2, lines 15-18) discloses that the organic resin is thermosetting.

► With respect to claim 11, Applicant Admitted Prior Art discloses (fig. 12, page. 2) a manufacturing method of a semiconductor device, comprising:

bonding a first supporting substrate (102) to a top surface of a semiconductor wafer (104), a first wiring (107) being formed on the top surface;

dividing the semiconductor wafer (104) into a plurality of semiconductor dice by etching the semiconductor wafer (104) along a dicing line from a back surface of the semiconductor wafer (104);

bonding a second supporting substrate (103) to a back surfaces of the plurality of semiconductor dice through a resin layer (105a);

forming a groove to expose a portion of the first wiring by cutting the second supporting substrate (103), the resin layer (105a), and the first supporting substrate (102) along the dicing line from a surface of the second supporting substrate, the groove reaching inside the first supporting substrate;

forming a second wiring (110) connected to the exposed portion of the first wiring (107) and extending over the surface of the second supporting substrate (103);

forming a protection film comprising an organic resin (epoxy resin) on a surface of the second wiring; and

forming an opening (the location of a ball shaped conductive terminal 106) in the protection film at a predetermined position to expose the second wiring (110).

Applicant Admitted Prior Art fails to disclose forming the protection film (epoxy resin) by spray coating method. However, Tanaka discloses that the protection film (epoxy resin) (119C) can be formed by spray coating method (see fig. 20, col. 13, lines 27-31). Therefore, it would have been obvious to the skilled in the art to use spray coating method as taught by Tanaka into the process of Applicant Admitted Prior Art because the spray coating is easy to control and well coated with even surface.

Allowable Subject Matter

5. Claims 2, 3, 6, 7, 12, 13, 15 are allowed.

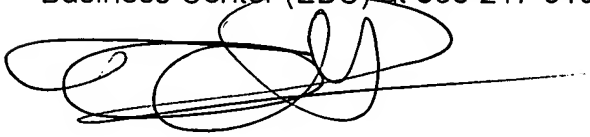
6. The following is an examiner's statement of reasons for allowance: the prior of record fails to disclose the combination of the process steps of forming a semiconductor device recited in the base claims 2, 6 and 12, including the process step of forming a cushioning portion on the second supporting substrate by spray coating.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thanhha Pham
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